CROS3 Readout System

Electronics Department

St. Petersburg Nuclear Physics Institute
Catchina, Russia

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Abstract:

- Complete On-Chamber Multiwire Coordinate Detector System
- Programmable Thresholds, Delays and Gates
- Time Distribution Measurement for Hit Wires within Gate
- High Density, Low Power Packaging
- Low Cost Per Channel
- Interfaces to PCI and Ethernet
- 40 MHz Readout
- Reduced Cabling

Overview

CROS3 is a prototype of complete Coordinate Readout Operating System, which is under design at PNPI to be used for fast readout of the coordinate detectors. The system is based on the experience gained with previous CROS Systems. The six different types of coordinate detectors have been readout by CROS2 in E781 experiment at Fermilab [1] and one type of coordinate detector has been readout in SPES-4π experiment at Saclay [2]. CROS3 contains the circuitry to amplify, discriminate, delay, latch, encode and readout the coordinate detector signals, all on a camber-mounted card. High performance and simplicity are achieved through the use of just 16-channel amplifier-discriminator ASIC [3] and high density Xilinx FPGA [4]. Host PCI controller and driver card provide readout and control of the system.

The specific features of CROS3 are:

- Continuous digitization of the input data stream;
- Fast clocked circuitry providing usable digital delay. The delay value is programmable within 256 steps. The step value is dependent of the experiment requirements. The range is 2.5 ns or 10 ns;
- Time distribution of hits within adjustable gate is available for readout. The gate value is programmable within 256 slices. The range is from 2.5 ns or 10 ns;
- LVDS differential signaling interconnect technology providing 40 MHz readout rate;
- Optical link technology for long distance data path;
- PCI interface to the host processor located on the standard PC motherboard;
- LVDS Trigger Bus to provide an Interface to the rigger Logic;

Functional Description

The physical packaging of this system is dependent on the experimental requirements and is designing to be easily modified to accommodate different chamber designs. Fig. 1 shows the system implementation based on the hex-width 96-channel wire block of MWPC, designed already at PNPI.

Six on-chamber mounted Amplifier/Discriminator (AD_16M) cards mate with Digitizing / Delay/ Readout (DDR_96) card via just six PCB connectors. No cable runs for these interconnections. Eight DDR_96 cards (768 wires in total) are interconnected together via LVDS copper CROS3 Databus. The last DDR_96 card in the databus chain contains an optical link transmitter for long distance interconnection to the CROS3 System Interface (CSI) card located on the PCI-bus of the dedicated computer motherboard. Six CSI cards can be installed in the computer motherboard to provide in total 4500-wire readout. The external Trigger Logic connected to the CSI Cards via LVDS Trigger Bus to control the data tacking according to real beam conditions. Upon the system Trigger is occurred the sparse readout cycles are started in DDR_96 cards in parallel. After the sparse encoding process is done the readout is started via LVDS databus and optical link to form six readout streams to the memory buffers, which are located into CSI cards. The memory buffers are then readout via PCI-bus to the host processor.

The Ethernet and VGA both optimize the computer motherboard. It allows the system to be integrated to the remote Data Acquisition and Slow Control.

1. AD_16M Card

The Card is based on 16-channel amplifier-discriminator ASIC [3]. The preamplifier – shaper is optimized for good timing resolution by sensing the first few electrons from the initial ionization in the chamber. The high-threshold discriminator is driven by the initial signal from the amplifier. The threshold level is adjustable from 10% to 70% of a nominal MIP signal. The resulting pulse serves as the enable for the precision time discriminator. The precision time discriminator consists of a constant-fraction shaper and a low-level discriminator. The constant-fraction shaping is done by adding the differential amplifier signal and the corresponding delayed and inverting signal. The resulting pulse is further amplified and delivered to the input of a low level zero-crossing discriminator. The zero crossing point corresponds to approximately half the rise time of the input signal. The threshold of the low-level discriminator is used for adjusting the start time of the output pulse. The design specifications for the preamp-shaper-discriminator circuits are listed below:

- Size 2.8" x 3.1"
- Number of channels 16;
- Power voltage +5.5V - +6V;
- Current 0.1A;
- Input impedance 40 Ohm equivalent;
- Minimum input signal 10 fC;
- Maximum input signal 1 pC;
- Minimum threshold 7fC;
- Maximum threshold 150 fC;
- Signal propagation time 100 ns;
- Dead time 80 ns;
- ASIC is implemented as 1.5 μm Bipolar-CMOS.
- Equivalent input noise (rms) is 0.5 fC at 0 pF (1.7 fC at 200 pF).
- Shaper peaking time is 30 ns.
- Shaped waveform is semi-gaussian with two exponent tail cancellations.
- Nominal input charge (i) is 142 fC ($8.8 \cdot 10^5$ e's).
- Transfer function (gain) is 5-mV/ fC (differential output).
- Two-threshold discriminator: high threshold used as enable, low threshold zero crossing disc driven by const-trac shaped pulse.
- High-level threshold adjustable from 20 – 500 mV.
- Discriminator slewing time is 2 ns.

2. DDR_96 Card

- Wire input receiver and digitizer;
- Programmable delay;
- Programmable gate;
- CROS3 LVDS Databus interface
- Optical Link interface.

The Digitizing/ Delay/ Readout (DDR_96) card is a 96-channel wire input receiver card designed for coordinate detector applications. Each card accepts 96 differential LVDS inputs.

The raw input data is digitized in coincidence with 100 MHz clock. The FIFO Delay takes digitized data and provides delay for each channel accounting for trigger logic delay. Two clocks – Write Clock and Read Clock, control the delay process and the preamble delay between both clocks is the value of the total delay. The extremely delay range is 2.5 ns to 640

ns in 2.5 ns step. The FIFO Gate takes the delayed data and provides time lapse accounting for gate value. Two clocks – Read Clock and Gate Clock, control the gate process and the preamble delay between both clocks is the value of the total gate. When the trigger is occurred the data is reading out from the FIFO Gate to provide the hit sparse encoding. Each hit successive DDR_96 sends the data to the CROS3 Databus. The readout rate is 40 MHz. The formatted data is then sent via Optical Link with rate at 800 Mb/sec.

A 96-bit pattern may be downloaded into input Test Register; allowing selected inputs to be transferred through the DDR_96. This ability allows the encoding logic to be completely tested.

Two fast clock options to control FIFO write/read process are possible: external Front Clock and Custom Clock from CROS3 Databus.

DDR_96 Specifications

Inputs

IN1 – IN6: 96 differential LVDS inputs via six 20-pair PCB connectors. Minimum input pulse width 10 ns.

Clock: NIM Level input. Input impedance 50 Ohm. Selection of Custom Clock and Front Clock via programmable jumper; the selected clock is using for digitizing and fast write/read process into clocked FIFO.

Trigger: NIM Level input. Input impedance 50 Ohm. Selection of Custom Trigger and Front Trigger via programmable jumper, the digitized selected clock pulse initiates sparse data scan slice by slice within gate. Minimum pulse width is 10 ns.

Inputs/ Outputs

P1: 40 Pins custom connector. Contains 8 data lines, 3 address, and 8 control lines. LVDS
differential signals.

J2: Infineon Optical Connector.

Digitizing

100 MHz **–** clock to digitize input pulses.

Delay

Range: 2.5 ns – 640 ns (2.5 ns step)
10 ns – 2560 ns (10 ns step)

Gate

Range: 2.5 ns – 640 ns (2.5 ns step)
10 ns – 2560 ns (10 ns step)

Double Pulse Resolution: 10 ns (max).

General:

Power Requirements: <1.5 A at +3.3V, 200mA at –5V.
Packaging**:** 9cm x 15 cm.

3. CSI Card

- Interface to Optical Link
- Interface to PCI Bus
- Interface to Trigger Logic

The Model CSI is a CROS3-PCI Interface designed as a small size card to install on the PCI Bus of the dedicated computer. Serves as the system interface and data buffer to store the several trigger events. The buffer size is 512 x 16 bit words.

P1 - 26 pin connector for the LVDS Trigger bus communications.

J2 – Infineon Optical Connector.

General
Power requirements: < 1A at +3.3V
Packaging: 9 cm x 12 cm

4. Trigger Rate

The trigger rate can be calculated as follows:

$TR = (0.4 + 0.01 \cdot G + 0.05 \cdot H)\ \mu s,$

G – the number of slices per gate
H – the number of hits per 768 bits within gate.

5. References

[1] FNAL E781 (SELEX) proposal (unpublished), July 1993: J.Russ, "SELEX – Hadroproduction of Charm Baryons out to Large xF", presented at "Productionand Decay of Hyperons, Charm and Beauty Hadrons", Strasbourg, September 1995.
[2] 278- The Spes4π project, News from Saturne N21 – November 1997.
[3] www.pnpi.spb.ru/ofve/red/products/cmp16_g.pdf
[4] Xilinx Spartan II FPGA.User manual.

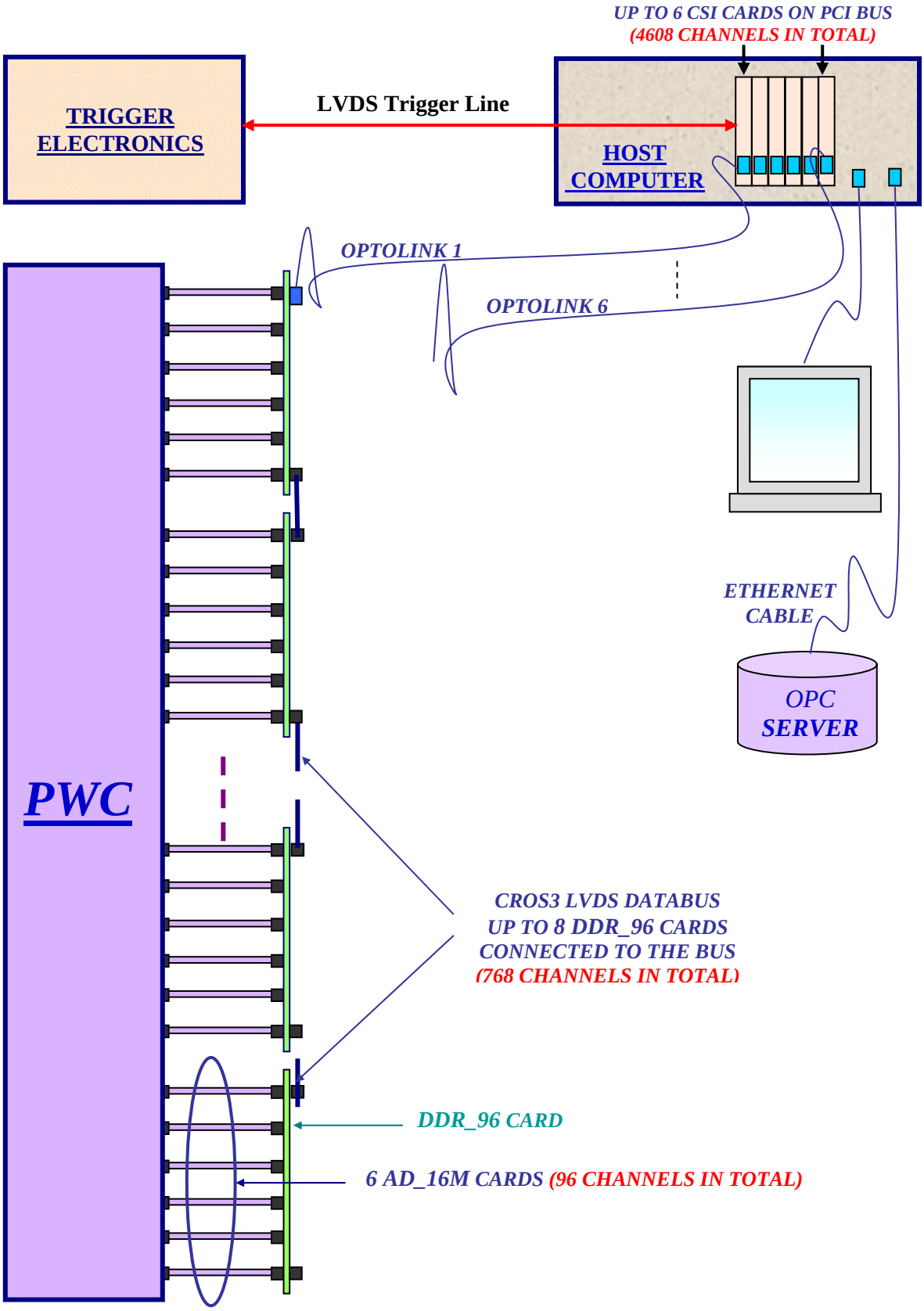

Fig.1 CROS3 System Configuration