CROS-3L – COORDINATE READOUT SYSTEM (LHCb TEST STAND VERSION)

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The design and development of the CROS-3 series is in the scope of interest of the LHCb Test Stand, which is constructed specially for tests of LHCb muon chambers [1]. We present a CROS-3L version, which has been designed and used for the LHCb Test Stand.

The block-diagram of the system is illustrated by Fig. 1 and includes:

- 4-channel front-end digitizer (ADF-L);
- 16-channel concentrator (CCB16);
- system buffer (CBS-B).

The analog part of the ADF-L is based on discrete elements performing chamber signal amplification and shaping, as well as pulse discrimination with peaking time 15 ns and operational threshold ≤ 15 fC. The digital part is implemented in a Xilinx Spartan-3 FPGA that performs both the time digitization and readout tasks. The delay range compensates trigger latency of up to 2.5 μs in 10 ns steps. The finest time bin resolution is 2.5 ns, the maximum number of time slices being 255. The amplitude digitization per each channel is performed by 10-bit ADC at a 100 MHz rate. The readout is performed over a STP CAT5 cable at a 100 Mb/s rate.

The CCB16 collects data from up to 16 digitizers into temporary buffers, which are read out to the CBS-B via an optical fiber at a 2.0 Gb/s. The CBS-B is implemented as a universal PCI card. The electronics modules of the system are illustrated by Figs. 2–4. Figure 5 shows the LHCb muon chamber equipped by CROS-3L electronics.

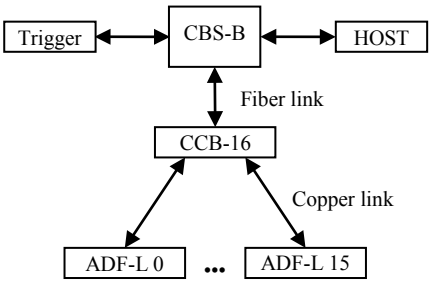

Fig. 1. CROS-3L set-up

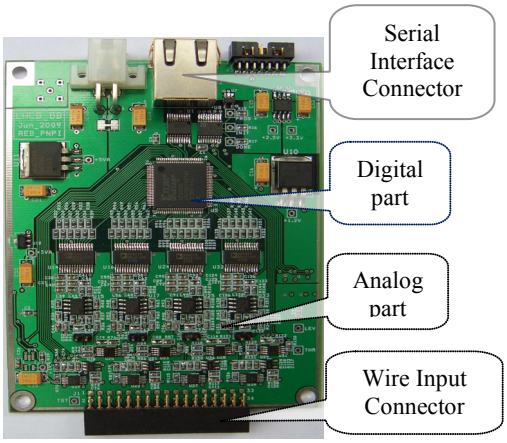

Fig. 2. ADF-L digitizer module

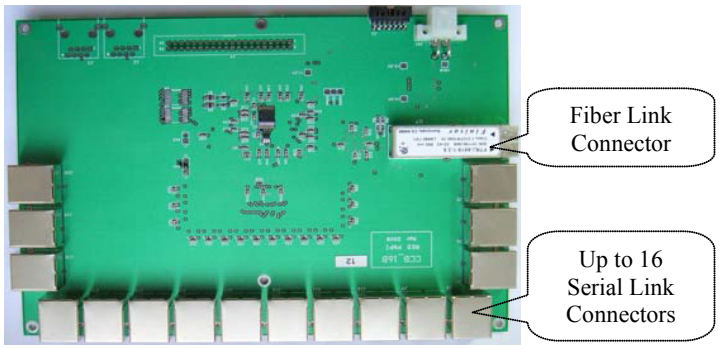

Fig. 3. CCB-16 concentrator module

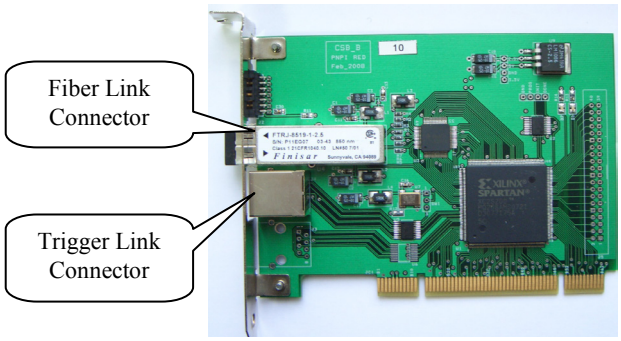

Fig. 4. CBS-B system buffer module

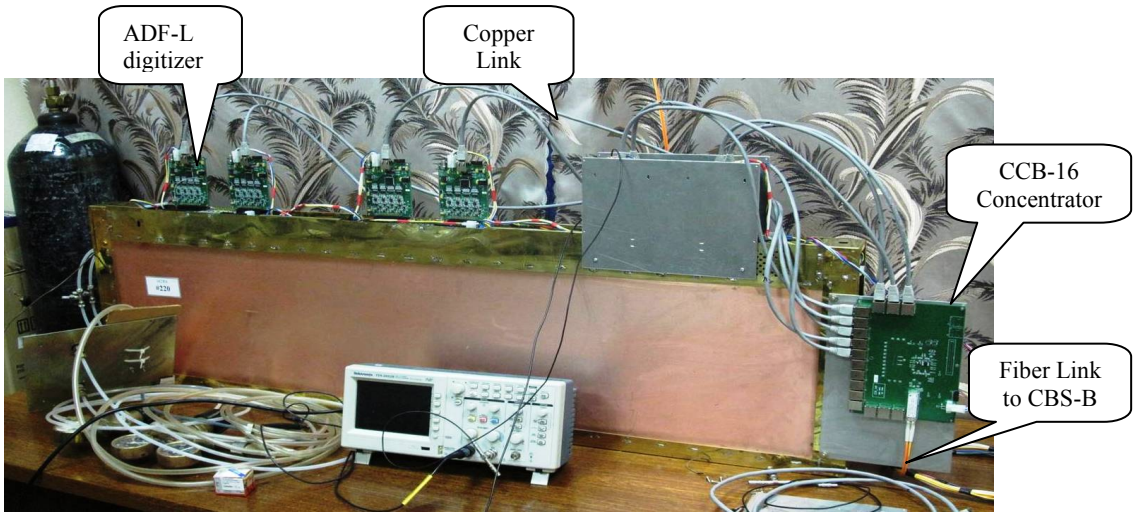

Fig. 5. LHCb muon chamber equipped by CROS-3L electronics at the Test Stand

The CROS-3L modules have the following features:

- the digitizers and the concentrator are mounted directly on the chamber;
- each digitizer amplifies, discriminates and pipelines input signals in parallel at a 100 MHz rate;
- when the system trigger occurs, the sparse encoding within the gate is started at a 400 MHz rate to collect data in parallel into a temporary buffer located in the digitizers;
- when the sparse encoding is over, the readout process is started over serial links at a 100 Mb/s rate to collect the sparse compacted data into a temporary buffer located in the concentrator;
- finally, the data are collected into the system buffer over the fiber link at a 2 Gb/s rate;
- fiber and copper links are used for the system trigger to be sent and the system constants such as the delay and gate values to be downloaded into the digitizer.

Reference

1. High Energy Physics Division, Main Scientific Activities 2002–2006, Gatchina (2007).